Five Level Inverter Fed Squirrel Cage Induction Motor Drive with Reduced Number of Power Elements

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Abstract: A topology for four switch five level inverter fed squirrel cage induction motor drive was presented in this paper. The three phase five level inverters is realized by cascading a three single phase inverter with output voltage phase sequence 120 degree lagging each other. Multi carrier sinusoidal pulse width modulation was used as a gate drive for the proposed inverter topology. The frequency of the reference wave determines switching time of MOSFET Switches. The proposed five level inverter configuration entail lesser number of switching devices as compared to the conventional five level inverter. Similarly, power supply requirement also less when compared to the conventional inverter drives.

Keywords: Multi carrier pulse width modulation (PWM); Four Switch Five level Inverter(FSFLI), Three Phase Squirrel Cage Induction Motor, Total Harmonic Distortion.

Introduction

Paper [1] proposes an improved single phase five level PWM inverter. In this paper firing signal for proposed inverter can be generated by comparing the reference signal with two carrier waves. Both having the same frequency and in phase with each other but two different offset levels. Paper [2] suggest the design of control scheme for a Nine Level Neutral Point C/H bridge inverter interfaced with the grid through an LCL filter. This Inverter topology produces the Nine level output waveform with low harmonic contents because of LCL filter. In five-level neutral-point clamped (NPC) H-bridge PWM inverter, a five level output voltage can be obtained by combining the three level outputs from both legs of the inverter. By choosing the phase of reference and carrier signal, a three-level output can be obtained. This inverter show signs of superior harmonics suppression property and leaving the multiples of the fourth order harmonics. Gating signal can be generated by comparing the triangular carrier wave with the sinusoidal reference wave[3]. In Paper [4], recommend the Model Predictive Direct Torque Control (MPDTC) which is used to reduce the converter's switching losses and improves the torque's Total Harmonic Distortion (THD). They introduced the MPDTC and applied to a five-level converter for driving the high frequency induction machine. By using MPDTC technique, they reduce the switching loss and Total harmonic distortion by fifty percentages. In Paper [5], they offer the PWM techniques with multi carrier for a 5-level Neutral Point Clamped (NPC) inverter. In that paper, they are using a new inverter topology for a 3-phase coupled inductor. This suggested inverter performance is mainly dependent on the PWM strategies. The use of the PWM techniques is reduction of current ripple and losses in the inductor side. In general, the conventional inverter fed induction machines rotor current and voltage quality is low due to the presents of harmonics in inverter output voltage. So there is a significant amount of energy losses due to the harmonics. This problem was overcome in Paper [6] by implementing the nine level inverter as a energy supply. While increasing the number of level in multi level inverter produce the high quality of output profile for induction motor drive. As previously discussed, harmonic losses are the important things in high power applications like AC drive. It should be reduced before applying to induction motor drive. Paper [7], they characterized the harmonic content by loss factor. They introduced the three PWM strategies for the three level inverters. Paper [8] proposes the five levels and seven level inverter fed induction motor drive system. Both the levels can be obtained by same two H Bridge circuit. The harmonic analysis was done for both the topologies and comparative analysis was shown. It clearly depict when number of levels was increased gradually the harmonic content also reduced. Paper [9] proposed that three phase three level inverters reduces the medium voltage drives especially used to reduce the harmonic content. They are verifying their model for 7.5 HP, 400 V squirrel cage induction motor drive system. Its used to increase no of steps of a induction motor step voltage its leads to reduce the dv/dt applied to the machine terminal. The Proposed [10] three phase five level topology having the 18 MOSFET switches. It reduces the convention Neutral Point Clamped inverter which is having the 18 clamping diodes and also it reduces 5 flying capacitor compared to the conventional flying capacitor which is using 6 capacitor. Hence proposed inverter reduces the circuit complexity.

Five Level Inverter

Proposed Five Leve Inverter Cicuit Model

The Fig. 1 shows the proposed model of single phase five level inverter which comprises of four MOSFET switches and single DC Source. The advantage of proposed inverter is reduced number of power switches over conventional 5 level inverters. Generally Multi Level Inverters are widely used because of its lowest harmonic contents in its output voltages. Due to the reduced harmonic contents requirement of output filter also reduced.

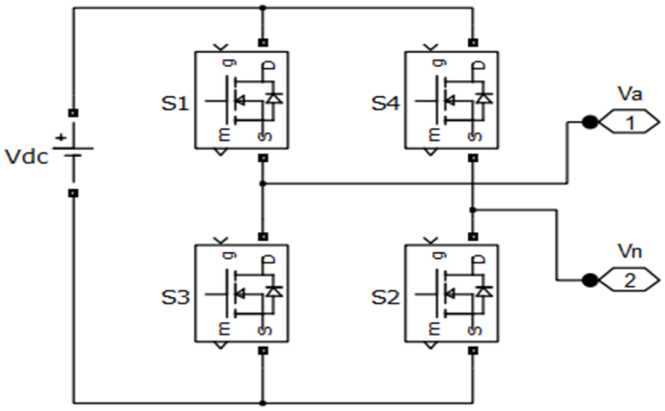
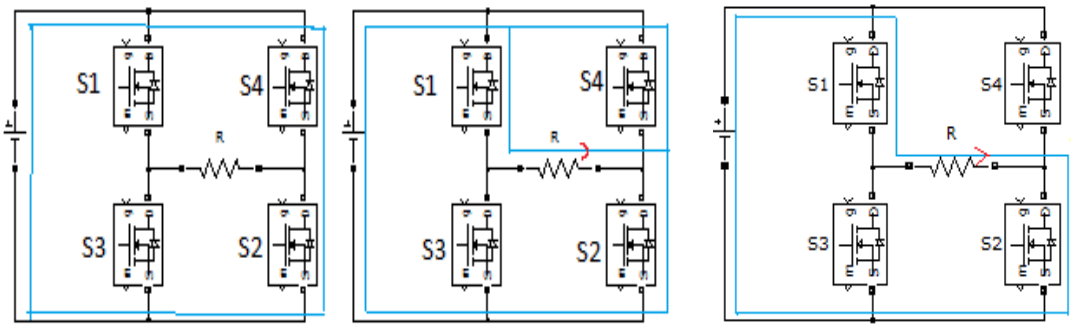


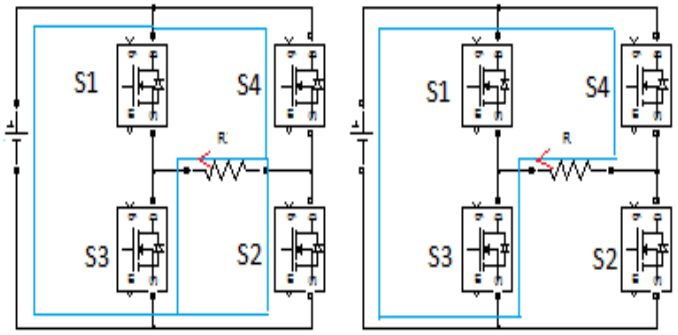
Figure 1. Proposed Four Switch 1 Phase Five Level Inverter Circuit Simulink Model

Operation of Proposed Inverter

The below shown Table 1depict the switch status of various levels of output voltage. For producing the Zero output voltage, the switches S1 and S3 are in OFF status and S2 and S4 are in ON status. So the current is circulating through the DC source, Switches S2 and S4. There is no current is flowing through the Load until the changes of the next triggering patterns. The next level of output $V_{DC}/2$ can be obtaining by giving the firing pulse to the switch S2.The Current flow direction is shown in the Fig. 2(b). The maximum voltage level V_{DC} can be obtained by giving the firing pulses to the switches S1 and S2. The current flow direction is shown in the Fig. 2(c). Voltage level $-V_{DC}$ can be obtained by making the switch S2 in ON status. The current flow direction is shown in the Fig. 2(d). The next level of voltage $-V_{DC}$ can be obtained by making switches S3 and S4 in ON status. The Current flow direction is shown the Fig. 2(e). The Fig. 3 shows the five level inverter simulation output voltage waveform. The harmonic analysis was done for this inverter output voltage. The THD value for this output wave form is 16.83%. The Fig. 4 shows the hardware image of the proposed single phase four switch five level inverter and Fig. 5 shows the hardware output stored by DSO.



(a) (b) (c)



(d) (e)

Figure 2. Five Level Inverter Operation Modes (a) 0 V (b) V_{DC}/2 V (c)V_{DC}V (d) -V_{DC}/2 V (e) -V_{DC}V

Table 1. Switching Table

V_{AC}	SWITCHES STATE			
	S1	**S2**	**S3**	**S4**
V_{DC}	ON	ON	OFF	OFF
V_{DC}/2	ON	ON	OFF	ON
0	OFF	ON	OFF	ON
-V_{DC}/2	OFF	ON	ON	ON
-V_{DC}	OFF	OFF	ON	ON

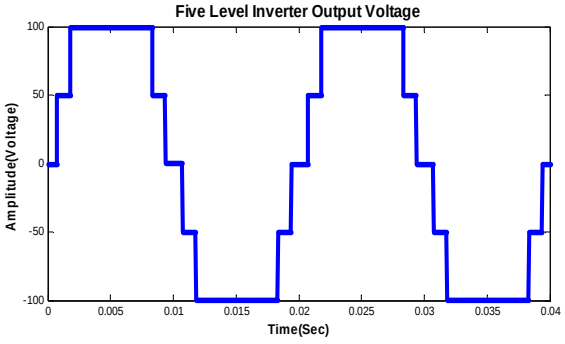


Figure 3. Proposed FLI Simulation Output Voltage Waveform

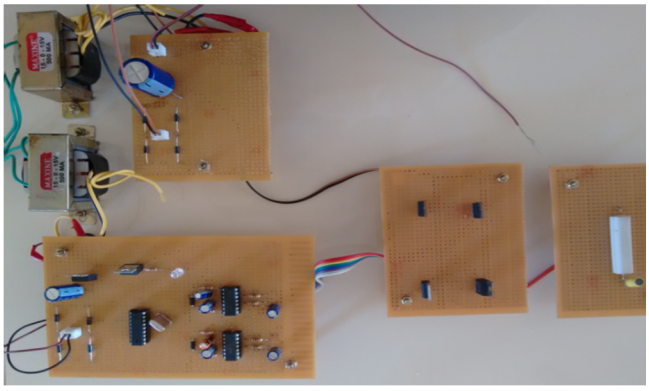


Figure 4. Hardware Image of Proposed FLI .

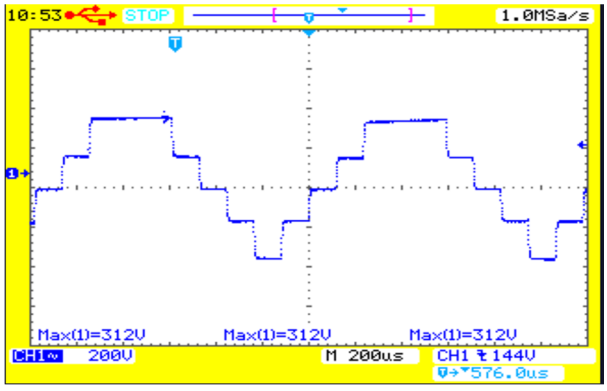


Figure 5. Proposed FLI Hardware Output Voltage Waveform

PWM Switching Strategy

The Switching pattern of the proposed inverter is generated by comparing the modulating wave which is a pure sinusoidal wave having the frequency of 50Hz with the four triangular carrier waves. The four triangular carrier waves having the same frequency and amplitude. The first two carrier waves having the same phase sequence but different offset levels. Similarly the next carrier waves having the same phase sequence but different offset levels.

The PWM pulse generation circuit consists of four carrier waves and one reference wave. Each carrier wave is shifted with the amplitude of AC with the other carrier waves. The firing pulses for the switches S1 and S2 can be generated when the amplitude of the reference wave is greater than the amplitude of the second and fourth carrier waves. In the same way the firing pulses for the Switches S3 and S4 can be generated when the amplitude of the reference wave is less than the third and first carrier waves respectively. The firing patterns for the five level inverter power switches shown in the Fig. 6.

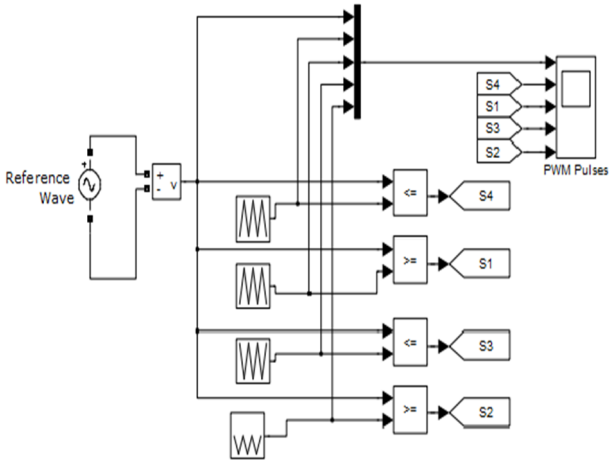


Figure 6. PWM Generation for 1 phase Five Level Inverter

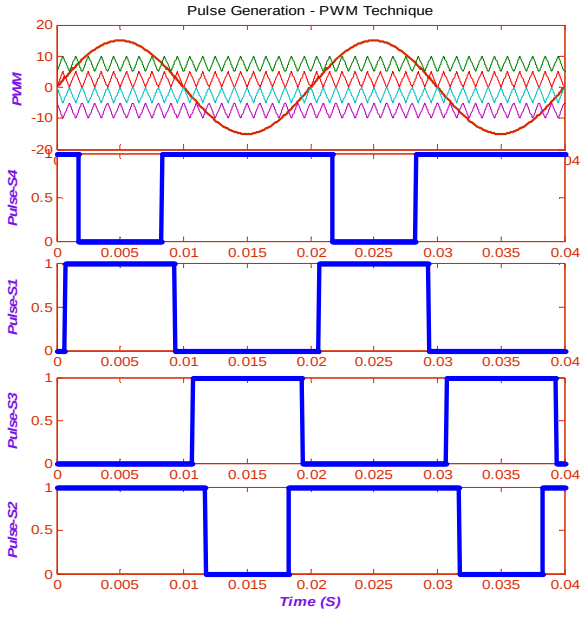


Figure 7. PWM Switching Pattern for Proposed Single Phase FLI

Three Phase Five Level Inverter Fed Induction Motor Derive

The proposed five level inverter was implemented with MOSFET as a switching elements and was tested with a 5.4 HP(4KW), 400 V, 1430 RPM, 50 HZ squirrel cage induction motor. The simulation was done using MATLAB 7.10.0 (R2010a)/ Simulink and corresponding simulation output was plotted. The Fig. 10 shows the simulink model for three phase five level inverter fed squirrel cage induction motor drive. The DC supply used for each single phase five level inverter is 200 V. The Fig. 8 shows the phase voltage of induction motor and Fig. 3 shows the single phase five level inverter pole voltage. FFT analysis was done for stator voltage, stator current and rotor speed of the squirrel cage induction motor drive. The gate drive system used for three phase five level inverter uses the below given reference wave as modulating signal for each phase of a power switches.

$$V_{aref} = V_m \sin \omega t$$
$$V_{bref} = V_m \sin (\omega t - 120)$$
$$V_{aref} = V_m \sin (\omega t - 240)$$

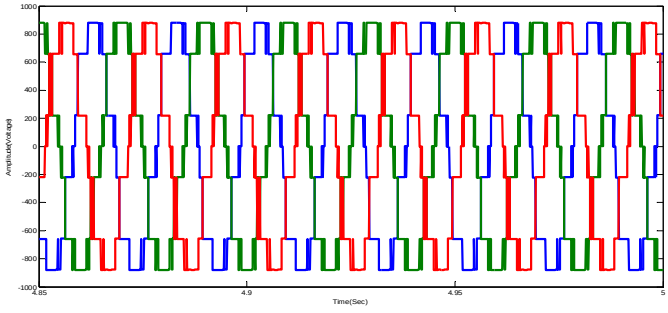


Figure 8. Three Phase Five Level Inverter Output Voltage Waveform

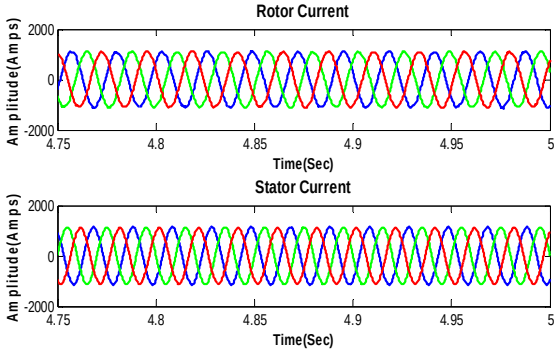


Figure 9. Stator and Rotor Current Profile of Multi Level Inverter fed three phases Induction Motor

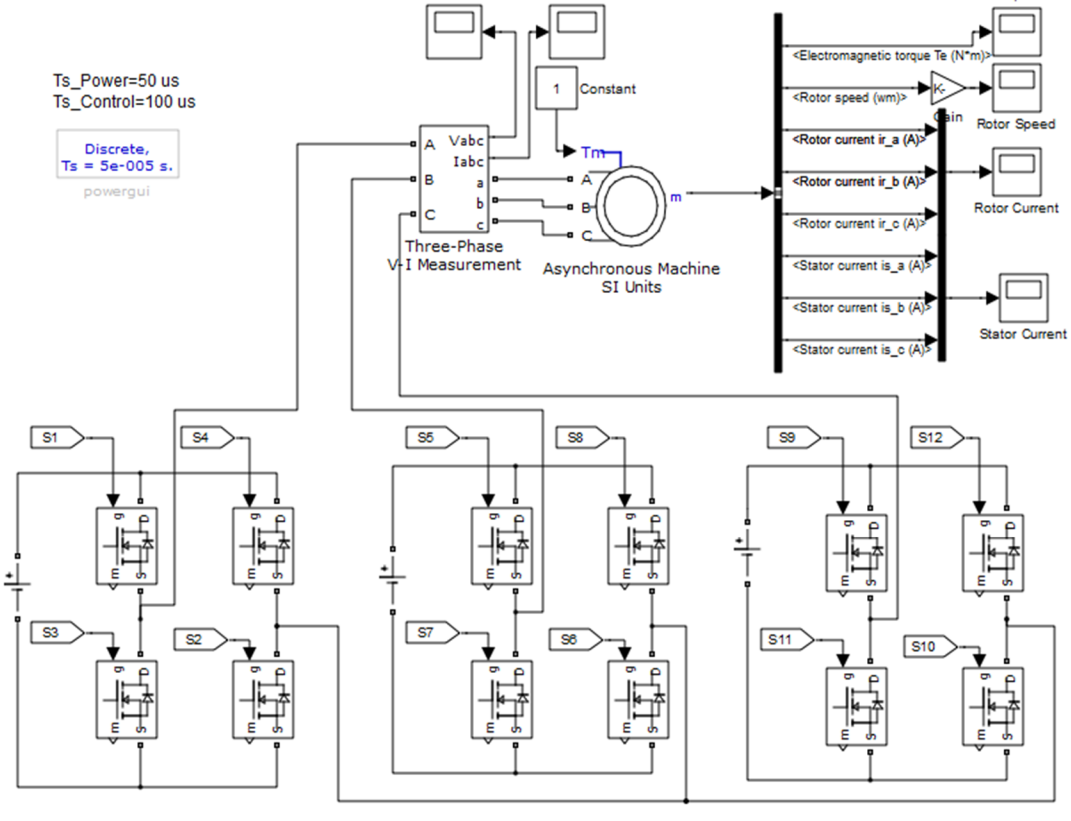


Figure 10. Simulink Model for Three Phase Five Level Inverter fed Squirrel Cage Induction Motor

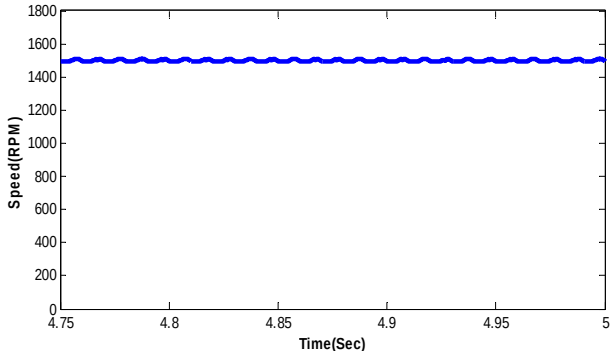


Figure 11. Rotor Speed of Multi Level Inverter fed three phases Induction Motor

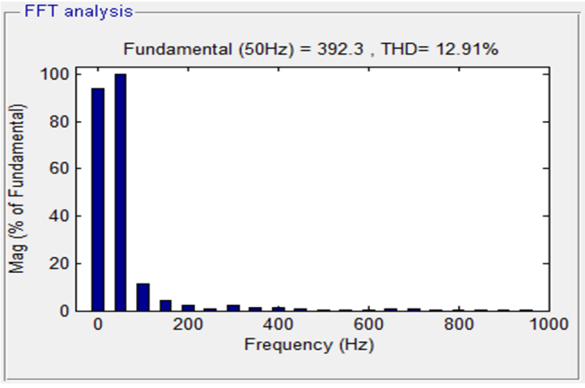


Figure 12. FFT analysis for Torque

Conclusion

The Proposed four switch five level inverter drive system can be used in high voltage industrial drive with minimum amount of harmonic content than the conventional speed drives. In this paper we have discussed about design and simulation of the 3φ five level inverter fed squirrel cage induction motor drive system. FFT analysis was done for the inverter output voltage, stator current, stator voltage and rotor speed of the induction motor .Four Carrier signal was used to generate the firing signal for MOSFET switches of proposed single leg of the 3φ five level inverter. The proposed inverter cost is very less compared to other inverter topology due to the less number of power elements.

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